IEEE 754, FPUs and Other Animals

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- IEEE p754 committee created, with most of the big industry players taking part
- MATLAB's creator Dr. Cleve Moler used to advise foreign visitors not to miss the US's two most awesome spectacles: the Grand Canyon, and meetings of IEEE p754

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- Only going to refer to IEEE 754-2008, and ignore decimal floating point as not many FPUs support them.

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- Taken to its logical extreme, the binary point is completely to the left: $0.6875 = 1 \cdot 2^{-1} + 0 \cdot 2^{-2} + 1 \cdot 1^{-3} + 1 \cdot 1^{-4}$

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- Note that this Q15, Q31 etc. can represent -1.0, but cannot represent +1.0

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- So the sign is a bit, the exponent is a signed number to take the multiplier of 2 by, and each bit in the mantissa is the amount of that decreasing power of two.

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  - Exact 1, but no zero!

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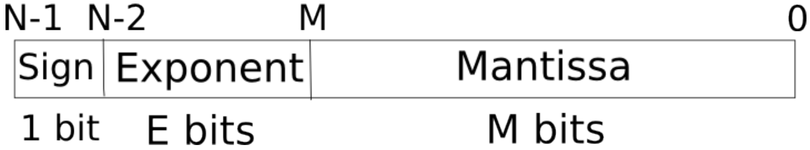

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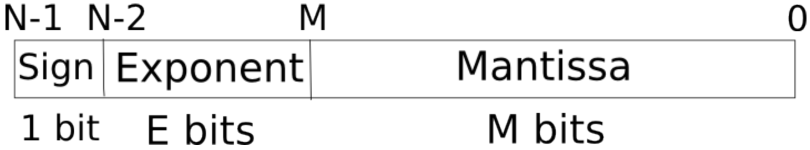

- Where N is the width of the format (e.g. 32)
- IEEE 754 defines three binary formats:
  - binary32 (single), N=32, E=8, M=23, bias=127
  - binary64 (double) , N=64, E=11, M=52, bias=1023
  - binary128, N=128, E=15, M=112, bias=16383
- Additionally, under the arbitrary precision, there is often:
  - binary16 (half), N=16, E=5, M=10, bias=15

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- Mantissa = b0101010101
  - $= 2^{-2} + 2^{-4} + 2^{-6} + 2^{-8} + 2^{-10}$
  - = 0.25 + 0.0625 + 0.015625 + 0.00390625 + 0.0009765625
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- Final answer = +1x0.25x1.3330078215 = 0.3332519553725
- Which is about as close to a 1/3 as it can get

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  - In this case, the always assumed 1 is actually 0, and the normalized exponent is maximum negative of the precision
  - How an FPU handles subnormal numbers is determined by version of the FPU, state of the control registers, and in some cases IMPLEMENTATION DEFINED. Thankfully, not the phase of the moon

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  - By default, all standard IEEE 754 floating point operations which produce NaNs only produce Quiet NaNs

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- There is a fifth optional mode, commonly used in decimal, but not in binary floating point - round to nearest, ties away from zero

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  - Some other edge cases

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  - Square root of a negative number
  - Some other edge cases
- Division by zero

Exceptions (1/2)

- IEEE 754 defines five exceptions
- A floating point exception does not necessarily mean a processor exception
- Invalid operation:
  - Performing an operation on a Signalling NaN
  - Adding or subtracting when both operands are an infinity
  - Dividing 0 by 0, or an infinity by an infinity
  - Square root of a negative number
  - Some other edge cases
- Division by zero
  - The output of the operation is the correctly signed infinity

Exceptions (2/2)

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  - The output of the operation is non-zero, but smaller than the format can represent. This is called tinniness
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  - Output would be finite but bigger than the format can hold
  - Depending on rounding, output can either be biggest finite number of the format, or an infinity
- Inexact
  - The output of the operation means that neither the desired mantissa nor desired exponent can be represented by the format
  - Nearly always paired with an Underflow or Overflow

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- atan2 is notorious for its edge conditions, and is classic example of where signed zero is required

Appendix